

REMARKS

The present application was filed on June 8, 2000 with claims 1-20. Claims 1-20 remain pending. Claims 1, 6, 13, and 20 are independent claims.

In the outstanding Office Action dated July 7, 2003, the Examiner: (i) rejected claims 1-20 under 35 U.S.C. §112, first paragraph; (ii) rejected claims 1 and 3-5 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,905,667 to Lee (hereinafter "Lee"); (iii) rejected claim 1 under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 3,646,332 to Suzuki (hereinafter "Suzuki") in view of Lee; and (iv) rejected claims 6-9, 11-16 and 18-20 under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 5,943,251 to Jiang et al. (hereinafter "Jiang") in view of Lee.

In response to the Office Action, Applicant amends claims 1, 6, 13 and 20 in an effort to expedite the application through to issuance.

With regard to the rejection of claims 1-20 under 35 U.S.C. §112, first paragraph, Applicant asserts that such claims are patentable for at least the reasons provided below. Claim 1 has been amended so that it no longer recites that the dynamic logic is without inversion of intermediate signals prior to a final stage. Instead, claim 1 recites that the dynamic logic is without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. Support for this amendment can be found in FIGS. 1 and 4 and their respective descriptions in the specification. Further, regarding the expressions for the binary output signal S(n), in boolean logic, the expression provided by the Examiner in the final Office Action is functionally equivalent to the expressions for S(n) provided on page 3, line 5, of the specification and in claim 2. Accordingly, withdrawal of the rejection to claims 1-20 under 35 U.S.C. §112, first paragraph, is therefore respectfully requested. 

With regard to the rejection of claims 1 and 3-5 under 35 U.S.C. §102(b) as being anticipated by Lee, Applicant asserts that such claims are patentable for at least the reasons that independent claim 1, from which claims 3-5 directly depend, is patentable.

Lee discloses an adder that includes a static logic block, a first dynamic inverter logic block, a dynamic logic block, and a second dynamic inverter logic block for generating a sum through a sum output node. Lee describes a dynamic logic version of an adder gate that uses a combination of inverting clock signals and short circuit current paths to conditionally discharge a dynamic node.

This solution consumes excess power through the dc current path of the pullup device MN5 and MN71 in FIG. 5, with the pull-down trees. Lee also uses two clocks, CLK and inverted clock CLKB, to prevent a pre-discharge of the dynamic node NODE52. The outputs SUM and CARRY can be in a high-impedance floating state when CLK is low and neither the SUM or CARRY is evaluated and a HIGH signal. This creates a noise sensitivity problem.

Independent claim 1 of the present invention was amended to more clearly set forth the invention and recites a circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. Support for this amendment can be found in FIGS. 1 and 4 and their respective descriptions in the specification. Lee discloses the inversion of signals driving one or more dynamic nodes associated with the dynamic logic through the inversion of its CARRY and SUM signals. Accordingly, withdrawal of the rejection to claims 1 and 3-5 under 35 U.S.C. §102(b) is therefore respectfully requested.

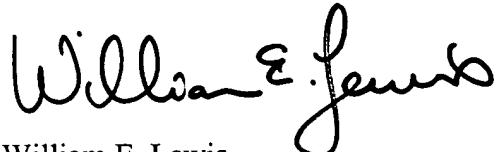
With regard to the rejection of claim 1 under 35 U.S.C. §103(a) as being obvious over Suzuki in view of Lee, Applicant asserts that the claim is patentable for the reasons presented above. Accordingly, withdrawal of the rejection to claim 1 under 35 U.S.C. §103(a) is therefore respectfully requested.

With regard to the rejection of claims 6-9, 11-16 and 18-20 under 35 U.S.C. §103(a) as being obvious over Jiang in view of Lee, Applicant asserts that such claims are patentable for at least the reasons that independent claims 6, 13 and 20, from which claims 7-9, 11, 12, 14-16, 18 and 19 directly or indirectly depend, are patentable. Claims 6, 13 and 20 have been amended so that they recite the limitation that dynamic logic is provided without inversion of signals driving one or more dynamic nodes associated with the dynamic logic. As acknowledged by the Examiner, Jiang does not disclose dynamic logic. Further, as described above, Lee discloses the inversion of signals driving dynamic nodes associated with the dynamic logic. Accordingly, withdrawal of the rejection of claims 6-9, 11-16 and 18-20 under 35 U.S.C. §103(a) is therefore respectfully requested.

Attorney Docket No. YO999-369

In view of the above, Applicant believes that claims 1-20 are in condition for allowance, and respectfully request withdrawal of the §112, §102(b) and §103(a) rejections.

Respectfully submitted,



Date: October 7, 2003

William E. Lewis
Attorney for Applicant(s)
Reg. No. 39,274
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY. 11560
(516) 759-2946